IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Yongjun Hu
Title: STRUCTURES AND METHODS TO ENHANCE FIELD EMISSION IN FIELD EMITTER DEVICES
Attorney Docket No.: 303.607US1

PATENT APPLICATION TRANSMITTAL

BOX PATENT APPLICATION
Assistant Commissioner for Patents
Washington, D.C. 20231

We are transmitting herewith the following attached items and information (as indicated with an "X"):

X Utility Patent Application under 37 CFR § 1.53(b) comprising:
- X Specification (37 pgs, including claims numbered 1 through 85 and a 1 page Abstract).
- X Informal Drawing(s) (13 sheets).
- X Signed Declaration (3 pgs).
- X Check in the amount of $4,426.00 to pay the filing fee.

X Assignment of the invention to Micron Technology, Inc. (2 pgs) and Recordation Form Cover Sheet.
X Check in the amount of $40.00 to pay the Assignment recording fee.
X Return postcard.

The filing fee has been calculated below as follows:

	No. Filed	No. Extra	Rate	Fee
TOTAL CLAIMS	85 - 20 =	65	x 18 =	**$1,170.00**
INDEPENDENT CLAIMS	35 - 3 =	32	x 78 =	**$2,496.00**
[ ] MULTIPLE DEPENDENT CLAIMS PRESENTED				**$0.00**
BASIC FEE				**$760.00**
TOTAL				**$4,426.00**

Please charge any additional required fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938, Minneapolis, MN 55402 (612-373-6900)

Customer Number 21186

By: _____
Atty: D. C. Peter Chu
Reg. No. 41,676

"Express Mail" mailing label number: EL254618052US Date of Deposit: August 31, 1999
I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents, Box Patent Application, Washington, D.C. 20231.

By: Chris Hammond Signature: Chris Hammond

STRUCTURES AND METHODS TO ENHANCE FIELD EMISSION IN FIELD EMITTER DEVICES

Field of the Invention

The present invention relates generally to semiconductor integrated circuits. More particularly, it pertains to structures and methods to enhance electron emission in a field emitter device.

Background of the Invention

Recent years have seen an increased interest in field emitter displays. This is attributable to the fact that such displays can fulfill the goal of being consumer-affordable hang-on-the-wall flat panel television displays with diagonals in the range of 20 to 60 inches. Certain field emitter displays operate on the same physical principles as cathode ray tube (CRT) based displays. Excited electrons are guided to a phosphor target to create a display. The phosphor then emits photons in the visible spectrum. This method of operation for field emitter displays relies on an array of field emitter tips.

Although field emitter displays promise to provide better color and image resolution, one of their problems is that it is difficult to get the field emitter to emit electrons so as to strike the phosphor target to generate the display. Another problem is that video images on these displays tend to take on undesired viewing characteristics over a relative short period of time. These undesired characteristics might be caused by degradation of the field emitter display due to certain conditions near the vicinity of the field emitter displays. These issues raise questions about the commercial success of the displays in the marketplace.

Thus, what is needed are structures and methods to enhance the emission of electrons in field emitter displays while dealing with the degradation of the field emitter over time.

Summary of the Invention

The above mentioned problems with field emitter displays and other problems are addressed by the present invention and will be understood by reading and studying the following specification. Structures and methods are described which accord these benefits.

In particular, an illustrative embodiment of the present invention includes a field emitter display device. This device comprises at least one emitter having an implantation that releases electrons at a predetermined energy level. The implantation enhances the releasing of electrons. The implantation also acts to limit outgassing so as to inhibit the degradation of the at least one emitter. In one embodiment, this implantation is embedded in the surface of the emitter.

These and other embodiments, aspects, advantages, and features of the present invention will be set forth in part in the description which follows, and in part will become apparent to those skilled in the art by reference to the following description of the invention and referenced drawings or by practice of the invention. The aspects, advantages, and features of the invention are realized and attained by means of the instrumentalities, procedures, and combinations particularly pointed out in the appended claims.

Brief Description of the Drawings

Figures 1A-1C are a close-up illustration of an emitter tip according to one embodiment of the present invention.

Figure 2 is an illustration of energy levels of field emitters according to one embodiment of the present invention.

Figure 3 is a planar view of a portion of an array of field emitters according to one embodiment of the present invention.

Figures 4A-4G are planar views of a field emitter device during various

stages of fabrication according to one embodiment of the present invention.

Figures 5A-5H are planar views of a field emitter device during various stages of fabrication according to another embodiment of the present invention.

Figures 6A-6G are planar views of a field emitter device during various stages of fabrication according to another embodiment of the present invention.

Figure 7 illustrates a sample of commercial products using a video display according to one embodiment of the present invention.

Figure 8 is a block diagram that illustrates a flat panel display system according to one embodiment of the present invention.

Detailed Description

In the following detailed description of the invention, reference is made to the accompanying drawings which form a part hereof, and in which is shown, by way of illustration, specific embodiments in which the invention may be practiced. In the drawings, like numerals describe substantially similar components throughout the several views. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention.

The terms wafer and substrate used in the following description include any structure having an exposed surface with which to form the integrated circuit (IC) structure of the invention. The term substrate is understood to include semiconductor wafers. The term substrate is also used to refer to semiconductor structures during processing, and may include other layers that have been fabricated thereupon. Both wafer and substrate include doped and undoped semiconductors, epitaxial semiconductor layers supported by a base semiconductor or insulator, as well as other semiconductor structures well known to one skilled in the art. The term conductor is understood to include semiconductors, and the

term insulator is defined to include any material that is less electrically conductive than the materials referred to as conductors. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims, along with the full scope of equivalents to which such claims are entitled.

The term "horizontal" as used in this application is defined as a plane parallel to the conventional plane or surface of a wafer or substrate, regardless of the orientation of the wafer or substrate. The term "vertical" refers to a direction perpendicular to the horizontal as defined above. Prepositions, such as "on," "side" (as in "sidewall"), "higher," "lower," "over," and "under" are defined with respect to the conventional plane or surface being on the top surface of the wafer or substrate, regardless of the orientation of the wafer or substrate.

In the process of identifying ways to emit electrons, it was discovered that the physical characteristics of the field emitter itself might be affecting the emission of electrons. Additionally, it was discovered that the beam of emitted electrons is smaller in those field emitter displays suffering from image quality degradation. These degraded field emitters were found to be surrounded by substances and compounds near the vicinity of the field emitters. Because the emitted electrons are the product of the array of tips in the field emitter display, the tip is discussed in detail below.

Figure 1A shows an embodiment of an emitter tip according to an embodiment of the present invention. A field emitter device 120 includes a substrate 100, a cathode tip 101 formed on the substrate 100, gate insulator layer 102, gate lines 116, and a phosphorescent anode 127 in opposing position with respect to the cathode tip 101. The construction of those elements of the field emitter device 120 will be explained below in other figures.

The cathode tip 101 emits electrons in response to the presence of an

electromagnetic field. The phosphorescent anode 127 releases photons when the emitted electrons strike the surface of the phosphorescent anode 127. An array of cathode tips 101 and phosphorescent anodes 127 forms the field emitter display. Video images are shown on the display as a result of the input of visual signals being modulated by the array of cathode tips 101 and phosphorescent anodes 127.

The cathode tip 101 includes an implantation 118. This implantation 118 affects the physical characteristics of the cathode tip 101 to enhance the releasing of electrons. This will be discussed below. Without this implantation 118, a strong electric field can be used to coerce the cathode tip 101 to emit more electrons.

Figure 1B shows a method of increasing the emission of electrons through the use of a strong electric field. For illustrative purposes only, the cathode tip 101 is shown as a cone with base radius b and height h. For simplifying the analysis, a circular disk 122 of radius b with uniform surface charge density σ is assumed. This circular disk lies in the x plane with its center at the origin.

Since electrons are emitted at point P, the behavior of the electric field at point P is investigated. From Figure 1B, the contribution of the charges on opposite sides of the circular disk 122 to the electric field in the x direction is canceled. However, the contribution of charges to the electric field in the z direction is cumulative. Therefore, the electric field at point P contains only the component in the z direction.

It is understood from the science of electromagnetism that the electric field of point P measuring from circular disk 122 is given by the equation: $E_z = (\sigma/2\varepsilon)(1 - (h / (h^2 + b^2)^{1/2}))$. E_z is the electric field in the z direction, ε is the permitivity, h is the height of the cone 101, and b is the radius of the cone 101.

Therefore, the electric field is directly proportional to σ and inversely proportional to the radius b of the cone 101. Increasing the electric field would increase the emission of electrons. Thus to increase the emission of electrons,

more charges must be supplied because of σ; this would mean imposing a larger potential across the cathode tip 101. Another way to increase the emission of electrons would be to make the tip of the cathode tip 101 sharper; this is accomplished by making the radius b smaller.

Figure 1C shows the cathode tip 101 with the implantation 118. This implantation 118 enhances the releasing of electrons without the need to increase the strength of the electric field. However, in one embodiment, electron emission is further enhanced by using the implantation 118 with an increase in the strength of the electric field.

Another benefit of the implantation 118 is that it allows the cathode tip 101 to limit outgassing, which has deteriorating effects upon the field emitter. One way to understand the problem of outgassing is to look at a measurement called the work function. The work function is a quantity of energy that must be supplied to move the electron from the surface of the cathode tip 101. Electrons that are more tightly bound within the cathode tip 101 require more energy to move. Different materials have different work functions. The cathode tip 101 without the implantation 118 is a source of outgassed materials. These outgassed materials increase the bond that binds the electron in the emitter tip. Therefore, the work function of the cathode tip 101 without the implantation 118 is increased in the presence of outgassing. As a result, the size of the emitted electron beam is reduced.

Outgassed substances and compounds exist in the environment near the vicinity of the cathode tip 101. The anode 127, the site that releases photons upon contact by the emitted electrons from the cathode tip 101, is one source of the outgassing. Another source is the cathode tip 101. The outgassing may contain carbon-based compounds, oxygen, hydrogen, water, argon, nitrogen, moisture, and others. In the absence of implantation 118, these outgassed substances and compounds act against the cathode tip 101. Once the physical structure of the

emitter tip is degraded, the size of the emitted electron beam is correspondingly reduced.

The implantation 118 helps the cathode tip 101 to be stable to limit outgassing so as to inhibit degradation to the cathode tip 101. Stable is understood to mean the inclusion of resistance to forces that disturb or alter the chemical makeup or physical state of the cathode tip 101. In one embodiment, inhibit is understood to mean the inclusion of substantial resistance to the degradation of the cathode tip 101. In another embodiment, inhibit is understood to mean the inclusion of a complete prevention of degradation of the cathode tip 101.

Figure 2 is a graph of energy levels of a field emitter according to one embodiment of the present invention. The graph represents a potential barrier (or potential hill) 20 that has been lowered because of the presence of an energy quantity $q\Delta\phi$. An electron must climb to the top 28 of the potential hill to free itself from the field emitter tip to reach the phosphorescent anode.

The potential hill 20 includes Fermi level 22. This level is symbolically represented by E_F. E_F is derived from Fermi-Dirac statistical analysis. It is understood that E_F represents the symmetrical reference point for the probability that a quantity of charges would exist or not exist above and below E_F. For illustrative purposes in the present embodiment, E_F is a likely starting point for an electron to begin its ascent to the top 28 to free itself from the tip of the field emitter.

The level 24 (E_{v0}) is an energy level, without $q\Delta\phi$, that an electron must reach to free itself from the tip of the field emitter. However, in the presence of $q\Delta\phi$, the level E_{v0} is reduced to E_{v1}. At level E_{v1}, an electron may free itself with less effort from the tip of the field emitter to reach the phosphorescent anode 127.

The energy quantity $q\Delta\phi$ is composed of the magnitude of the electronic charge, q, and $\Delta\phi$. $\Delta\phi$ is a lowering mechanism that reduces the potential hill 20. In one embodiment, $\Delta\phi$ is described as $\Delta\phi = (qE / 4\pi\varepsilon_s)^{1/2}$,where:

$\Delta\phi$ is in volts.

q is in coulombs. q is the magnitude of the electronic charge.

E is in newtons per coulomb. E is the electric field.

ε_s is in coulombs per volt-meter. ε_s is the permitivity of the material of the emiter tip. In one embodiment, ε_s represents the permitivity of silicon.

Thus to lower the potential hill 20 to allow electrons to escape the field emitter tip, the quantity $q\Delta\phi$ should be increased. Since q is a constant, the controllable quantity is $\Delta\phi$. To increase $\Delta\phi$ would require either increasing the electric field E, decreasing the permitivity ε_s of the material of the emitter tip, or both. It is understood that ε_s is described as $\varepsilon_s = \varepsilon_r\varepsilon_0$, where:

ε_r is the relative dielectric constant of the material of the emitter tip.

ε_0 is in coulombs per volt-meter. ε_0 is the permitivity of free space.

To decrease the permitivity ε_s of the material of the emitter tip would require decreasing the relative dielectric constant ε_r since the permitivity of free space ε_0 is a constant. In one embodiment, the relative dielectric constant ε_r is the relative dielectric constant of silicon.

Another way to understand how emission of electrons can be eased is to improve the image force. An image force is created when negative charges are brought near the surface of the cathode tip's surface. Positive charges are attracted to such negative charges and will be induced under the surface of the cathode tip. Such induction creates a force that, when combined with an external electric field, would reduce the potential barrier. As previously mentioned, this potential barrier is the hill that electrons must escape to free themselves from the field emitter tip to reach the phosphorescent anode.

Yet another way to understand how emission of electrons can be eased is to increase the Schottky effect. This effect is realized when a semiconductor material is brought in contact with a layer of low relative dielectric constant material. In one embodiment, the Fermi level is moved so as to shorten the potential barrier

that the electrons must climb to free themselves from the tip of the field emitter. In another embodiment, the top of the potential barrier is lowered.

In yet another way to understand the emission of electrons, by affecting the lowering mechanism, affecting the image force, improving the Schottky effect, or lowering the dielectric of the field emitter, the energy level by which the electrons must be excited to free them from the electronic bond with the nucleus of the material of the cathode tip and move them from the cathode tip is reduced.

Figure 3 is a planar view of an embodiment of a portion of an array of field emitter devices including 350A, 350B, 350C, . . ., 350N, and constructed according to an embodiment of the present invention. The field emitter array 305 includes a number of cathodes, 301_1, 301_2, 301_3, . . ., 301_n, formed in rows along a substrate 300. A gate insulator 302 is formed along the substrate 300 and surrounds the cathodes. A number of gate lines 316 are on the gate insulator. A number of anodes including 327_1, 327_2, 327_3, . . ., 327_n are formed in columns orthogonal to and opposing the rows of cathodes. In one embodiment, the anodes include multiple phosphors. In another embodiment, the anodes are coated with phosphorescent or luminescent substances or compounds. Additionally, the intersections of the rows and columns form pixels.

Each field emitter device in the array, 350A, 350B, . . ., 350N, is constructed in a similar manner. Thus, only one field emitter device 350N is described herein in detail. All of the field emitter devices are formed along the surface of a substrate 300. In one embodiment, the substrate includes a doped silicon substrate 300. In an alternate embodiment, the substrate is a glass substrate 300, including silicon dioxide (SiO_2). Each field emitter device 350 includes a cathode 301 formed in a cathode region 325 of the substrate 300. The cathode 301 includes a polysilicon cone 301. In one exemplary embodiment, the polysilicon cone 301 includes an implantation 318.

A gate insulator 302 is formed in an insulator region 312 of the substrate

300. The cathode 301 and the gate insulator 302 have been formed, in one embodiment, from a single layer of polysilicon. A gate 316 is formed on the gate insulator 302.

An anode 327 opposes the cathode 301. In one embodiment, the anode is covered with light emitting substances or compounds that are luminescent or phosphorescent.

Figures 4A-4G show a process of fabrication for a field emitter device according to one embodiment of the present invention. Figure 4A shows the structure focusing on the cathode tip, after tip sharpening, following the first stages of processing. One with ordinary skill in the art would be familiar with these stages of processing.

Figure 4B shows the structure during an implantation of a dose of ions into a portion of the cathode tip 401. In one embodiment, the implantation is a shallow implantation using low energy. In another embodiment, the ions are implanted to form an implantation layer 418 at about 50 to 100 Angstroms from the surface of the portion of the cathode tip 401. In another embodiment, the dose of ions is a high dose that includes 10^{17} per square centimeter of ions. In another embodiment, the ion is one species of atomic oxygen, such as O^-. In another embodiment, the ion forms an oxide compound with the material of the cathode tip; in this embodiment, the ion includes O^{2-} ions. In another embodiment, the ion forms a superoxide compound with the material of the cathode tip; in this embodiment, the ion includes O^-_2 ions. In another embodiment, the ion forms a peroxide compound with the material of the cathode tip. In one embodiment, the implantation layer 418 that is formed is a silicon oxide layer; it is understood that the relative dielectric constant of the silicon oxide layer with bubbles or other imperfections is approximately 3.0 whereas the relative dielectric constant of silicon is about 12. In yet another embodiment, the ion is one species of atomic nitrogen. In a further embodiment, the ion is an ionic nitride. It is understood

that a compound of silicon nitride has a relative dielectric constant of about 7.5 whereas the relative dielectric constant of silicon is about 12.

Figure 4C shows the structure after the next sequence of fabrication stages. In one embodiment, an annealing process is used upon the cathode tip 401 to stabilize the ion implantation to form the implantation 418. The structure now appears as in Figure 4C. In one embodiment, the annealing process is a rapid thermal process using nitrogen. The temperature range for such a process is about 850 degrees Celsius to about 1000 degrees Celsius.

Figure 4D shows the structure following the next sequence of processing. The insulator 408 may be referred to as a gate insulator or grid dielectric. The insulator 408 is formed over the cathode tip 401 and the substrate 400. The regions of the insulator 408 that surround the cathode tip 401 constitute an insulator region 412 for the field emitter device.

Figure 4E shows the structure following the next stages of processing. A gate or gate layer 416 is formed on the insulator layer 408. The gate layer 416 includes any conductive layer material and can be formed using any suitable technique. One exemplary technique includes chemical vapor deposition (CVD).

Figure 4F shows the structure following the next stages of processing. Following deposition, the gate layer 416 undergoes a removal stage. In one embodiment, the gate layer 416 is removed until a portion of the insulator layer 408, covering the cathode tip 401, is revealed.

Figure 4G shows the structure after the next sequence of processing. Here a portion of the insulator layer 408 is removed from the surrounding of the cathode tip 401. The portion of the insulator layer 408 is removed using any suitable technique as will be understood by one of ordinary skill in the field of semiconductor processing and field emission device fabrication; one exemplary technique includes using reactive ion etching. The formation of the anode 427 is further formed opposing the cathode tip 401 in order to complete the field

emission device. The formation of the anode, and completion of the field emission device structure, can be achieved in numerous ways as will be understood by those of ordinary skill in the art of semiconductor and field emission device fabrication.

Figures 5A-5H show fabrication of a field emitter device according to one embodiment of the present invention. Figure 5A shows the structure focusing on the cathode tip, after tip sharpening, following the first stages of processing.

Figure 5B shows the structure following the next sequence of processing. The insulator 508 is also known as a gate insulator, or grid dielectric. The insulator 508 is formed over the cathode tip 501 and the substrate 500. The regions of the insulator 508 that surround the cathode tip 501 constitute an insulator region 512 for the field emitter device.

Figure 5C shows the structure following the next stages of processing. A gate or gate layer 516 is formed on the insulator layer 508. The gate layer 516 includes any conductive layer material and can be formed using any suitable technique. One exemplary technique includes chemical vapor deposition (CVD).

Figure 5D shows the structure following the next stages of processing. Following deposition, the gate layer 516 undergoes a removal stage. The gate layer 516 is removed using a suitable technique until a portion of the insulator layer 508, covering the cathode tip 501, is revealed; one exemplary technique includes chemical mechanical planarization.

Figure 5E shows the structure after the next sequence of processing. Here a portion of the insulator layer 508 is removed from the surrounding of the cathode tip 501. The portion of the insulator layer 508 is removed using any suitable technique as will be understood by one of ordinary skill in the field of semiconductor processing and field emission device fabrication; one exemplary technique includes a combination of a lift-off technique and reactive ion etching process.

Figure 5F shows the structure during an implantation of a dose of ions into a portion of the cathode tip 501. In one embodiment, the implantation is a shallow implantation using low energy. In another embodiment, the ions are implanted at about 50 to 100 Angstroms from the surface of the portion of the cathode tip 501. In another embodiment, the dose of ions is a high dose that includes 10^{17} per square centimeter of ions. In another embodiment, the ion is one species of atomic oxygen, such as O^-. In another embodiment, the ion forms an oxide compound with the material of the cathode tip; in this embodiment, the ion includes O^{2-} ions. In another embodiment, the ion forms a superoxide compound with the material of the cathode tip; in this embodiment, the ion includes O^-_2 ions. In one embodiment, the implantation layer 418 that is formed is a silicon oxide layer; it is understood that the relative dielectric constant of the silicon oxide layer is approximately 4 whereas the relative dielectric constant of silicon is about 12. In yet another embodiment, the ion is one species of atomic nitrogen. In a further embodiment, the ion is an ionic nitride. It is understood that a compound of silicon nitride has a relative dielectric constant of approximately 7.5 whereas the relative dielectric constant of silicon is about 12.

Figure 5G shows the structure after the next sequence of fabrication stages. In one embodiment, an annealing process is used upon the cathode tip 501 to stabilize the ion implantation to form the implantation 518. The structure now appears as in Figure 5G. In one embodiment, the annealing process is a rapid thermal process using nitrogen. In a further embodiment, the temperature range for such a process is about 850 degrees Celsius to about 1000 degrees Celsius.

Figure 5H shows the structure after the next sequence of processing. The formation of the anode 527 is further formed opposing the cathode tip 501 in order to complete the field emission device. The formation of the anode, and the completion of the field emission device structure, can be achieved in numerous ways as will be understood by those of ordinary skill in the art of semiconductor

and field emission device fabrication. The formation of the anodes, and completion of the field emission device itself, do not limit the present invention and as such are not presented in full detail here.

Figures 6A-6G show a process of fabrication for a field emitter device according to an embodiment of the present invention. Figure 6A shows the structure focusing on the cathode tip, after tip sharpening, following the first stages of processing. One with ordinary skill in the art would be familiar with these stages of processing.

Figure 6B shows the structure during the process of implantation of at least a portion of the cathode tip 601 with a layer of low relative dielectric constant material. In one embodiment, a uniform-step-coverage technique is used to apply a layer of the low relative dielectric constant material with uniform thickness. In one embodiment, the layer of low relative dielectric constant has a value less than about the relative dielectric constant of the material of the cathode tip 601. In another embodiment, the layer of low relative dielectric constant has a value less than about 50 percent of the relative dielectric constant of the material of the cathode tip 601. In another embodiment, the layer of low relative dielectric constant has a value less than about 5. In yet another embodiment, the layer of low relative dielectric constant has a value less than about 12.

Figure 6C shows the structure after the next sequence of fabrication stages. In one embodiment, a layer of silicon 606 is used to cover the layer 605. In another embodiment, the silicon layer 606 includes a thickness of 50 to 100 Angstroms. Having covered up the layer 605 with the layer of amorphous silicon 606, an implantation 618 is defined. In one embodiment, the layer of silicon 606 is continuous. In another embodiment, the layer of silicon 606 is a thin film, about 50 to 100 Angstroms. Reducing the thickness of the layer of silicon 606 tends to reduce outgassing within the vicinity of the cathode tip 601.

Figure 6D shows the structure following the next sequence of processing.

The insulator 608 may be referred to as a gate insulator or grid dielectric. The insulator 608 is formed over the cathode tip 601 and the substrate 600. The regions of the insulator 608 that surround the cathode tip 601 constitute an insulator region 612 for the field emitter device.

Figure 6E shows the structure following the next stages of processing. A gate, or gate layer 616, is formed on the insulator layer 608. The gate layer 616 includes any conductive layer material and can be formed using any suitable technique, such as sputtering or chemical vapor deposition.

Figure 6F shows the structure following the next stages of processing. Following deposition, the gate layer 616 undergoes a removal stage. In one embodiment, the gate layer 616 is removed until a portion of the insulator layer 608, covering the cathode tip 601, is revealed.

Figure 6G shows the structure after the next sequence of processing. Here a portion of the insulator layer 608 is removed from the surrounding of the cathode tip 601. The portion of the insulator layer 608 is removed using any suitable technique as will be understood by one of ordinary skill in the field of semiconductor processing and field emission device fabrication. One exemplary technique includes a combination of a lift-off technique and reactive ion etching.

The formation of the anode 627 is further formed opposing the cathode tip 601 in order to complete the field emission device. The formation of the anode, and completion of the field emission device structure, can be achieved in numerous ways as will be understood by those of ordinary skill in the art of semiconductor and field emission device fabrication. The formation of the anodes and completion of the field emission device do not limit the present invention and as such are not presented in full detail here.

Figure 7 shows exemplary video display products using an array of field emitter devices 708 in accordance with an embodiment of the present invention. The array of field emitter devices 708 are described and presented above in

connection with the above figures. In one embodiment, the video display product is a camcorder 702; the camcorder 702 includes a camcorder viewfinder incorporating an array of field emission devices. In another embodiment, the video display product is a flat-screen television 704 incorporating an array of field emission devices. In a further embodiment, the video display product is a personal appliance 706 incorporating an array of field emission devices. In all embodiments, the video display product includes a display screen for showing a video image.

Figure 8 is a block diagram that illustrates an embodiment of a flat panel display system 850 according to an embodiment of the present invention. A flat panel display includes a field emitter array formed on a glass substrate. The field emitter array includes a field emitter array 830 as described and presented above in connection with the above Figures. A row decoder 820 and a column decoder 810 each couple to the field emitter array 830 in order to selectively access the array. Further, a processor 840 is included which is adapted to receiving input signals and providing the input signals to address the row and column decoders 820 and 810.

Conclusion

Thus, structures and methods have been described to enhance electron emission and to limit outgassing in field emitter devices. The various embodiments can be operated in severe environments, such as in temperatures above room temperature, in space applications, and in aqueous environments. Additionally, the invention is especially appropriate for mobile applications since it can be operated with a low power supply.

Although the specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted

for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. It is to be understood that the above description is intended to be illustrative, and not restrictive. Combinations of the above embodiments and other embodiments will be apparent to those of skill in the art upon reviewing the above description. The scope of the invention includes any other applications in which the above structures and fabrication methods are used. Accordingly, the scope of the invention should only be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.

What is claimed is:

1. A field emitter display device, comprising:

at least one emitter having an implanted oxide layer that releases electrons at a predetermined energy level.

2. The device of claim 1, wherein the implanted oxide layer inhibits outgassing that includes moisture.

3. A field emitter display device, comprising:

at least one emitter having an implantation that releases electrons at a predetermined energy level, wherein the implantation lowers the potential barrier to enhance the releasing of electrons.

4. The device of claim 3, wherein the implantation is a layer underneath the surface of the at least one emitter.

5. A field emitter display device, comprising:

at least one emitter having an implantation that emits electrons at a predetermined energy level, wherein the implantation affects the lowering mechanism so as to enhance the emission of electrons.

6. The device of claim 5, wherein the implantation is a layer underneath the surface of the at least one emitter.

7. A field emitter display device, comprising:

at least one emitter having an implantation that releases electrons at a predetermined energy level, wherein the implantation affects the image force so as to enhance the releasing of electrons.

8. The device of claim 7, wherein the implantation is a layer underneath the surface of the at least one emitter.

9. A field emitter display device, comprising:

at least one emitter having an implantation that emits electrons at a predetermined energy level, wherein the implantation enhances the Schottky effect so as to enhance the emission of electrons.

10. The device of claim 9, wherein the implantation is a layer underneath the surface of the at least one emitter.

11. A field emitter display device, comprising:

at least one emitter having an implantation that releases electrons at a predetermined energy level, wherein the implantation decreases the dielectric effect of the at least one emitter to enhance the releasing of electrons.

12. The device of claim 11, wherein the implantation is a layer underneath the surface of the at least one emitter.

13. A field emitter display device, comprising:

at least one emitter having a layer that releases electrons at a predetermined energy level, wherein the layer enhances the releasing of electrons and the layer limits the outgassing so as to inhibit degradation of the at least one emitter.

14. The device of claim 13, wherein the layer is embedded in the surface of the at least one emitter.

15. A field emitter display device, comprising:

at least one emitter having a layer that releases electrons at a predetermined energy level, wherein the layer lowers the potential barrier to enhance the releasing of electrons and the layer limits the outgassing so as to inhibit degradation of the at least one emitter.

16. The device of claim 15, wherein the layer is embedded in the surface of the at least one emitter.

17. A field emitter display device, comprising:

at least one emitter having a layer that releases electrons at a predetermined energy level, wherein the layer affects the image force so as to enhance the releasing of electrons and the layer limits the outgassing so as to inhibit degradation of the at least one emitter.

18. The device of claim 17, wherein the layer is embedded in the surface of the at least one emitter.

19. A field emitter display device, comprising:

at least one emitter having a layer that emits electrons at a predetermined energy level, wherein the layer improves the Schottky effect so as to enhance the emission of electrons and the layer limits the outgassing so as to inhibit degradation of the at least one emitter.

20. The device of claim 19, wherein the layer is embedded in the surface of the at least one emitter.

21. A field emitter display device, comprising:

at least one emitter having a layer that releases electrons at a predetermined energy level, wherein the layer decreases the dielectric effect of the at least one emitter to enhance the releasing of electrons and the layer limits the outgassing so as to inhibit degradation of the at least one emitter.

22. The device of claim 21, wherein the layer is embedded in the surface of the at least one emitter.

23. A field emitter display device, comprising:

at least one emitter having a silicon oxide layer.

24. A field emitter display device, comprising:

at least one emitter having an oxide layer that releases electrons at a predetermined energy level.

25. A field emitter display device, comprising:

at least one emitter having an embedded silicon oxide layer.

26. The device of claim 25, wherein the embedded silicon oxide layer is formed by an implantation process.

27. A field emitter display device, comprising:

at least one emitter having an external coating and an embedded layer that releases electrons at a predetermined energy level, wherein the embedded layer limits outgassing to inhibit degradation of the at least one emitter and enhances the releasing of electrons.

28. A field emitter display device, comprising:

at least one emitter having an external coating and an embedded layer that releases electrons at a predetermined energy level, wherein the embedded layer limits outgassing to inhibit degradation of the at least one emitter and lowers the potential barrier to enhance the releasing of electrons.

29. A field emitter display device, comprising:

at least one emitter having an external coating and an embedded layer that releases electrons at a predetermined energy level, wherein the embedded layer limits outgassing to inhibit degradation of the at least one emitter and affects the lowering mechanism so as to enhance the emission of electrons.

30. A field emitter display device, comprising:

at least one emitter having an external coating and an embedded layer that

releases electrons at a predetermined energy level, wherein the embedded layer limits outgassing to inhibit degradation of the at least one emitter and affects the image force so as to enhance the releasing of electrons.

31. A field emitter display device, comprising:

at least one emitter having an external coating and an embedded layer that releases electrons at a predetermined energy level, wherein the embedded layer limits outgassing to inhibit degradation of the at least one emitter and improves the Schottky effect so as to enhance the emission of electrons.

32. A field emitter display device, comprising:

at least one emitter having an external coating and an embedded layer that releases electrons at a predetermined energy level, wherein the embedded layer limits outgassing to inhibit degradation of the at least one emitter and decreases the dielectric effect of the at least one emitter to enhance the releasing of electrons.

33. A field emitter display device, comprising:

at least one emitter having an implantation that releases electrons at a predetermined energy level, wherein the implantation reduces the potential barrier to enhance the releasing of electrons and inhibits degradation of the at least one emitter in the presence of the outgassing; and

a light-emitting target that radiates when the released electrons strike the light-emitting target.

34. The device of claim 33, wherein the light-emitting target is coated with luminescent matter.

35. The device of claim 33, wherein the light-emitting target is coated with phosphorescent matter.

36. A video display, comprising:

a display screen for showing a video image; and

an array of field emission devices capable of forming the video image, wherein the array of field emission devices comprises:

at least one emitter having an implantation that releases electrons at a predetermined energy level, wherein the implantation reduces the dielectric effect of the at least one emitter and is stable in the presence of the outgassing; and

a light-emitting target that radiates when the released electrons strike the light-emitting target.

37. A method for enhancing the emission of electrons in a field emitter device, comprising:

forming at least one tip behaving as cathodes in the field emitter device, the at least one tip emitting electrons at a predetermined energy level;

forming at least one phosphorescent target behaving as anodes in the field emitter device, the at least one phosphorescent target receptive to the emitted electrons; and

implanting the at least one tip with a layer having a reduced dielectric constant, the layer enhancing the emission of electrons and limiting the outgassing so as to inhibit degradation in the field emitter device.

38. The method of claim 37, wherein the method proceeds in the order presented.

39. The method of claim 37, wherein implanting the at least one tip with a layer comprises implanting with the layer that affects the image force so as to enhance the emission of electrons.

40. The method of claim 37, wherein implanting the at least one tip with a layer comprises implanting with the layer that improves the Schottky effect so as to enhance the emission of electrons.

41. A method of forming a field emission device, comprising:

forming an emitter tip on a substrate;

forming a substance on at least a portion of the emitter tip, wherein the substance decreases the dielectric effect of the emitter tip; and

forming an anode opposite the emitter tip.

42. The method of claim 41, wherein forming the substance comprises forming the substance that lowers the potential barrier to enhance the emission of electrons.

43. The method of claim 41, wherein forming the substance comprises forming the substance that affects the image force so as to enhance the emission of electrons.

44. The method of claim 41, wherein forming the substance comprises forming the substance that improves the Schottky effect so as to enhance the emission of electrons.

45. A method of forming a field emission device, comprising:

forming an emitter tip on a substrate;

implanting a substance to form a compound in at least a portion of the emitter tip, wherein the implanting reduces the dielectric effect of the emitter; and

forming an anode opposite the emitter tip.

46. The method of claim 45, wherein implanting the substance to form the compound comprises implanting the substance that lowers the potential barrier to enhance the emission of electrons.

47. The method of claim 45, wherein implanting the substance to form the compound comprises implanting the substance that affects the image force so as to enhance the emission of electrons.

48. The method of claim 45, wherein implanting the substance to form the compound comprises implanting the substance that improves the Schottky effect so as to enhance the emission of electrons.

49. A method of forming a field emission device, comprising:

forming an emitter tip on a substrate;

implanting oxygen ions in at least a portion of the emitter tip; and

forming an anode opposite the emitter tip.

50. The method of claim 49, wherein implanting oxygen ions comprises implanting O^- ions.

51. The method of claim 49, wherein implanting oxygen ions comprises implanting O^{2-} ions.

52. The method of claim 49, wherein implanting oxygen ions comprises implanting O^{-}_{2} ions.

53. The method of claim 49, wherein implanting oxygen ions comprises implanting a species of oxygen ions to form a silicon dioxide compound.

54. A method of forming a field emission device, comprising:

forming an emitter tip on a substrate;

implanting a predetermined dose of oxygen ions in at least a portion of the emitter tip; and

forming an anode opposite the emitter tip.

55. The method of claim 54, wherein implanting the predetermined dose of oxygen ions comprises implanting the predetermined dose of oxygen ions on the order of about 10^{17} per square centimeter.

56. The method of claim 54, further comprising annealing to stabilize the oxygen ions embedded in the emitter tip.

57. The method of claim 56, wherein annealing to stabilize the compound comprises annealing through a rapid thermal process using nitrogen.

58. The method of claim 56, wherein annealing occurs in a temperature greater than about 850 degrees Celsius.

59. The method of claim 56, wherein annealing occurs in a temperature less than about 1000 degrees Celsius.

60. The method of claim 56, wherein annealing occurs in a temperature greater than about 850 degrees Celsius and less than about 1000 degrees Celsius.

61. A method of forming a field emission device, comprising:

forming an emitter tip on a substrate;

implanting a predetermined dose of oxygen ions to form a compound in at least a portion of the emitter tip;

annealing to stabilize the compound embedded in the emitter tip; and

forming an anode opposite the emitter tip.

62. The method of claim 61, wherein implanting the predetermined dose of oxygen ions comprises implanting a desired dose of oxygen ions on the order of about 10^{17} per square centimeter.

63. The method of claim 61, wherein annealing to stabilize the compound comprises annealing through a rapid thermal process using nitrogen.

64. The method of claim 61, wherein annealing to stabilize the compound comprises annealing in a temperature greater than about 850 degrees Celsius and less than about 1000 degrees Celsius.

65. The method of claim 61, wherein the method proceeds in the order presented.

66. A method of forming a field emission device, comprising:

forming an emitter tip on a substrate;

implanting oxygen ions at a predetermined depth greater than about 50 Angstroms and less than about 100 Angstroms from the surface of the emitter tip;

annealing to stabilize the oxygen ions embedded in the emitter tip; and

forming an anode opposite the emitter tip.

67. The method of claim 66, wherein implanting oxygen ions comprises implanting a desired dose of oxygen ions on the order of about 10^{17} per square centimeter.

68. The method of claim 66, wherein annealing to stabilize the compound comprises annealing through a rapid thermal process using nitrogen.

69. The method of claim 66, wherein annealing to stabilize the compound comprises annealing in a temperature greater than about 850 degrees Celsius and less than about 1000 degrees Celsius.

70. A method of forming a field emission device, comprising:

forming an emitter tip on a substrate;

implanting a substance on at least a portion of the emitter tip so as to form an implanted layer having a relative dielectric constant less than about the relative dielectric constant of the emitter tip;

annealing to stabilize the implanted layer in the emitter tip; and

forming an anode opposite the emitter tip.

71. The method of claim 70, wherein implanting a substance comprises implanting a desired dose of oxygen ions on the order of about 10^{17} per square centimeter.

72. The method of claim 70, wherein annealing to stabilize the compound comprises annealing through a rapid thermal process using nitrogen.

73. The method of claim 70, wherein annealing to stabilize the compound comprises annealing in a temperature greater than about 850 degrees Celsius and less than about 1000 degrees Celsius.

74. The method of claim 70, wherein implanting the substance comprises implanting at a depth greater than about 50 Angstroms and less than about 100 Angstroms.

75. A method of forming a field emission device, comprising:

forming an emitter tip containing silicon on a substrate;

implanting a dose of oxygen ions of about 10^{17} per square centimeter on at least a portion of the emitter tip so as to create a relative dielectric constant of the emitter tip greater than about 3.0 and less than about 12;

annealing in nitrogen to form a layer of silicon oxide embedded at a depth

greater than about 50 Angstroms and less than about 100 Angstroms in the emitter tip using a rapid thermal process at a temperature greater than about 850 degrees Celsius and less than about 1000 degrees Celsius; and

forming an anode opposite the emitter tip.

76. A method of forming a field emission device, comprising:

forming an emitter tip containing silicon on a substrate;

implanting a dose of oxygen ions of about 10^{17} per square centimeters in at least a portion of the emitter tip;

annealing in nitrogen to form a layer of silicon dioxide embedded at a depth greater than about 50 Angstroms and less than about 100 Angstroms in the emitter tip using a rapid thermal process at a temperature greater than about 850 degrees Celsius and less than about 1000 degrees Celsius; and

forming an anode opposite the emitter tip.

77. The method of claim 76, wherein implanting the dose of oxygen ions comprises implanting oxygen ions to form a superoxide compound.

78. A method of forming a field emission device, comprising:

forming an emitter tip on a substrate;

implanting a species of nitrogen at greater than about 50 Angstroms and

less than about 100 Angstroms from the surface of the emitter tip;

annealing to form a compound containing the species of nitrogen embedded in the emitter tip; and

forming an anode opposite the emitter tip.

79. A method of forming a field emission device, comprising:

forming an emitter tip on a substrate;

implanting ionic nitride on at least a portion of the emitter tip;

annealing to form a compound containing nitride embedded in the emitter tip; and

forming an anode opposite the emitter tip.

80. A method of forming a field emission device, comprising:

forming an emitter tip on a substrate;

depositing a layer of low relative dielectric constant material over the emitter tip so as to enhance the emission of electrons;

depositing a layer of a substance over the layer of low relative dielectric constant material; and

forming an anode opposite the emitter tip.

81. The method of claim 80, wherein depositing the layer of low relative

dielectric constant material comprises depositing through a uniform-step-coverage technique to form a uniform thickness layer of the low relative dielectric constant material.

82. The method of claim 80, wherein depositing the layer of low relative dielectric constant material comprises depositing a layer of a material having a dielectric constant less than about 12.

83. The method of claim 80, wherein depositing the layer of the substance comprises depositing to form a thickness greater than about 50 Angstroms and less than about 100 Angstroms.

84. The method of claim 80, wherein depositing the layer of the substance comprises depositing an amorphous and continuous film of the substance.

85. The method of claim 80, wherein depositing the layer of the substance comprises depositing an amorphous and continuous film of silicon.

STRUCTURES AND METHODS TO ENHANCE FIELD EMISSION IN FIELD EMITTER DEVICES

Abstract of the Disclosure

Structures and methods to ease electron emission and limit outgassing so as to inhibit degradation to the electron beam of a field emitter device are described. In one method to ease such electron emission, a layer of low relative dielectric constant material is formed under the surface of the field emitter tip. Another method is to coat the field emitter tip with a low relative dielectric constant substance or compound to form a layer and then cover that layer with a thin layer of the material of the field emitter tip.

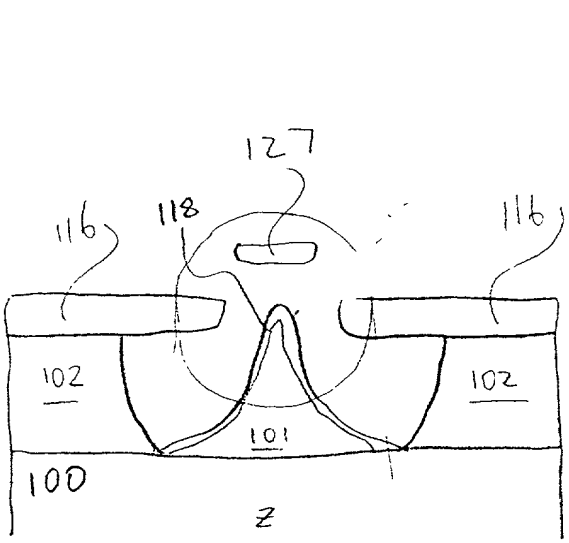

FIG. 1 A

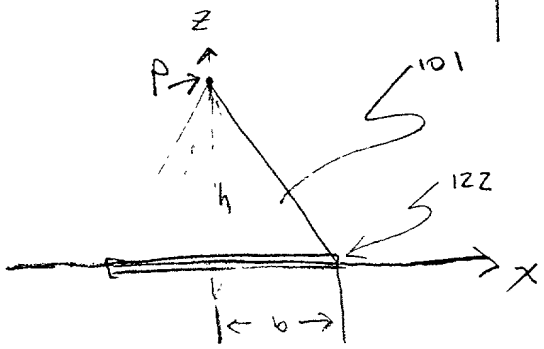

FIG 1 B

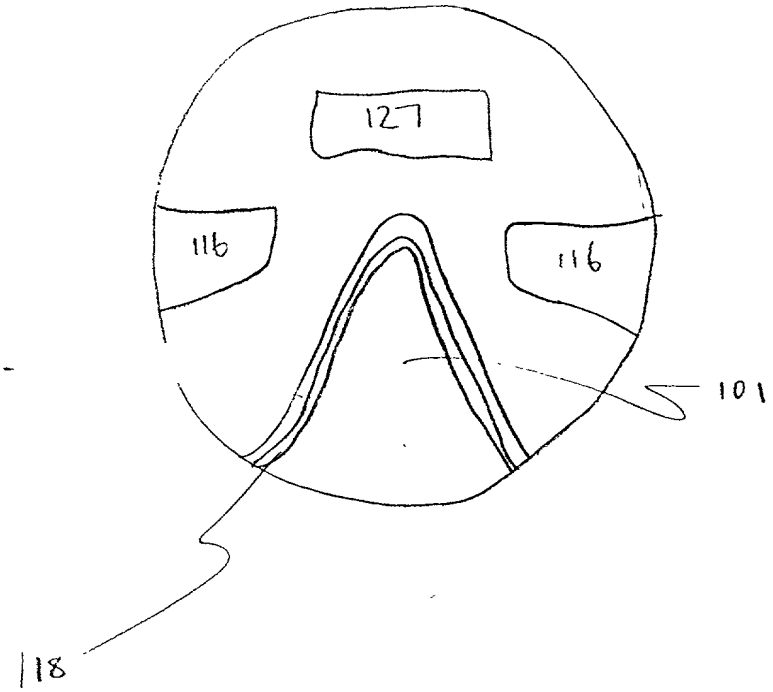

FIG 1C

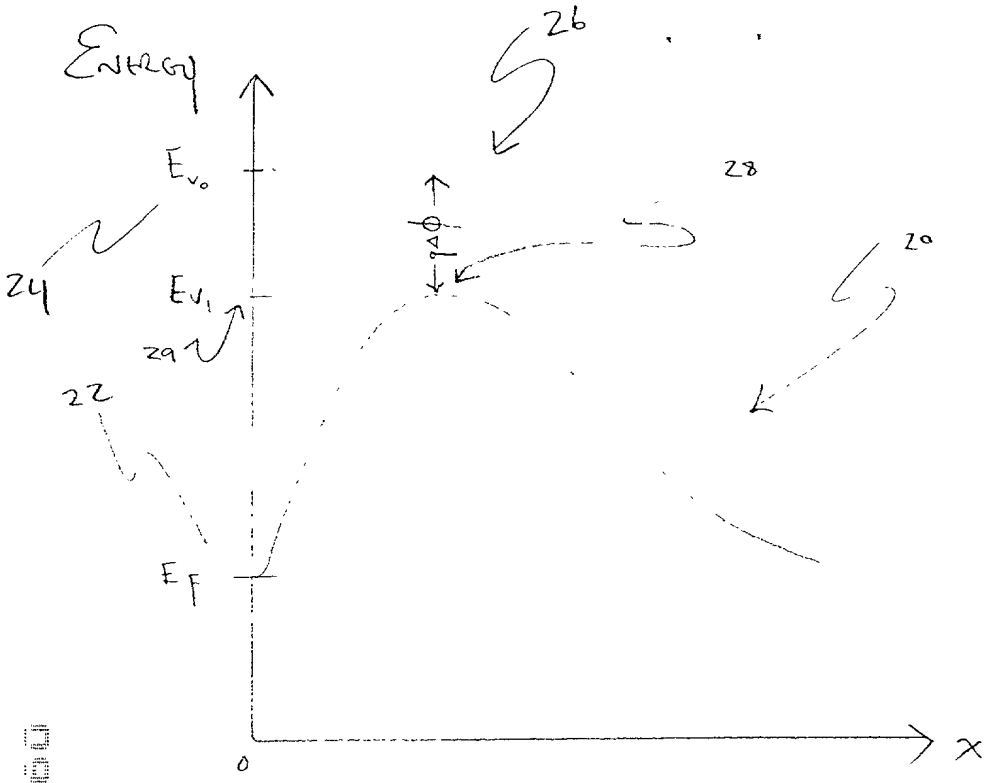

FIG. 2

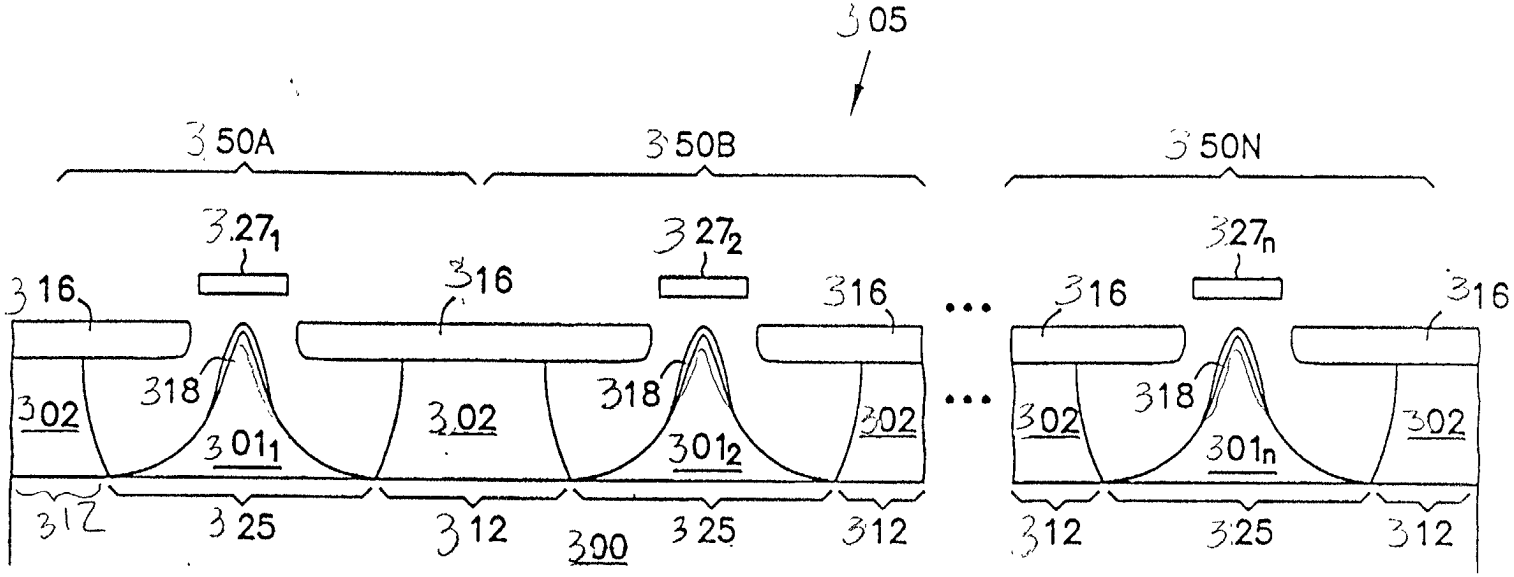

FIG. 3

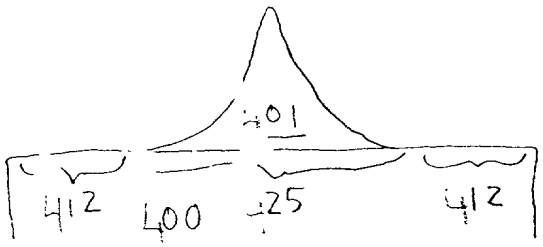

FIG.4A

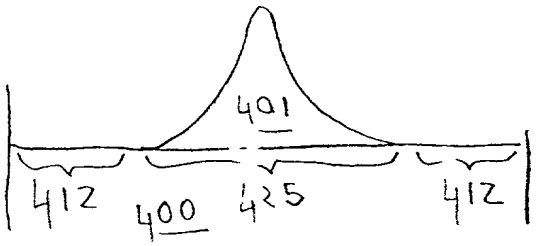

FIG.4B

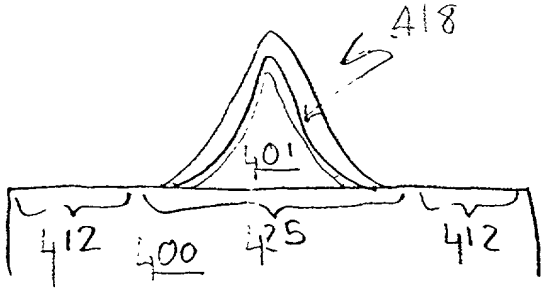

FIG. 4C

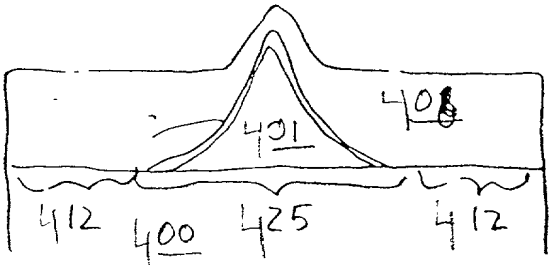

FIG. 4D

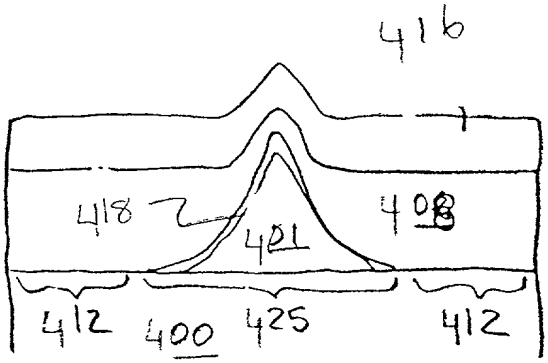

FIG. 4E

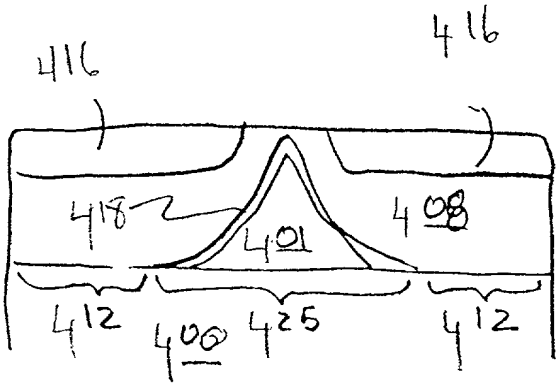

FIG. 4F

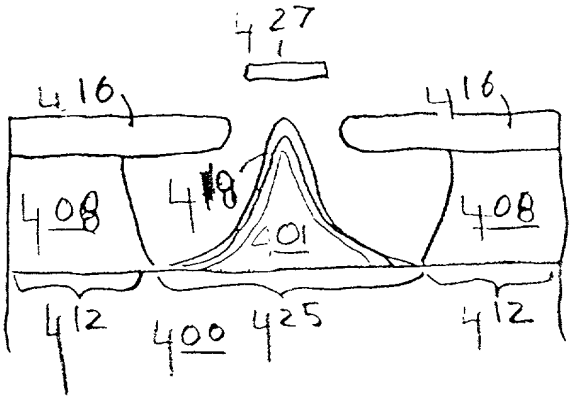

FIG 4G

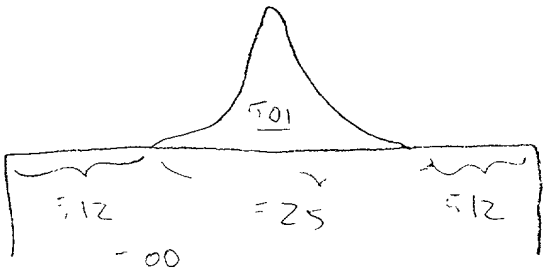

FIG 5A

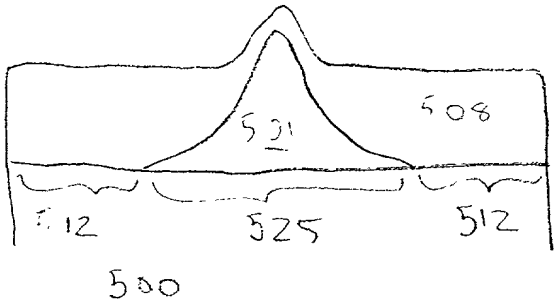

FIG. 5B

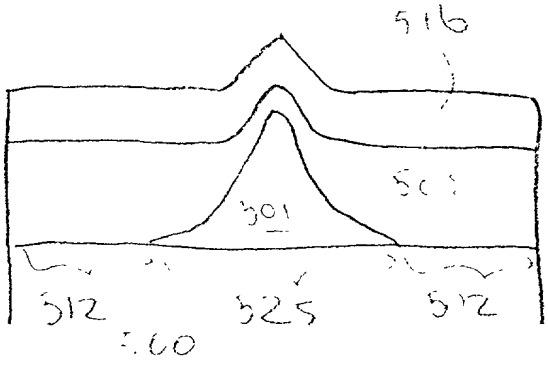

FIG. 5C

FIG 5D

FIG 5E

FIG 5F

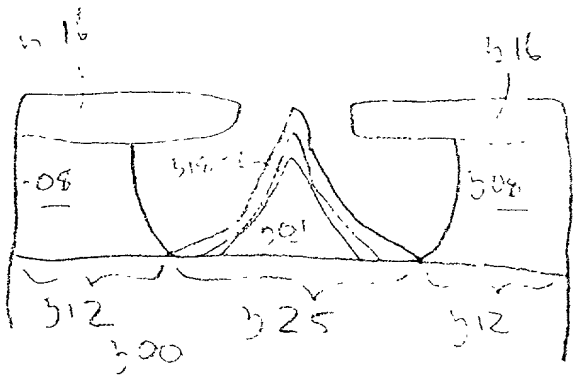
516
516
508
508
501
512
525
512
500

FIG 5G

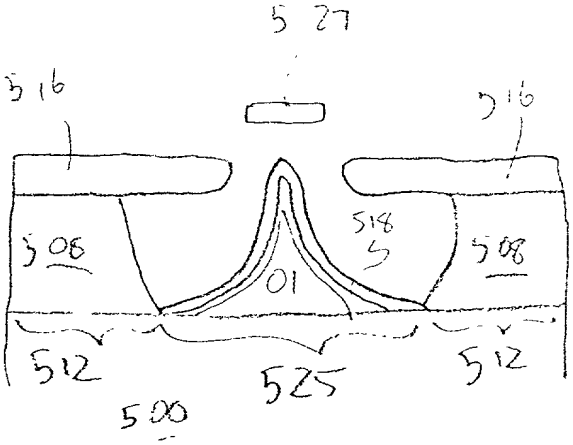
527
516
516
508
508
518
501
512
525
512
500

FIG 5H

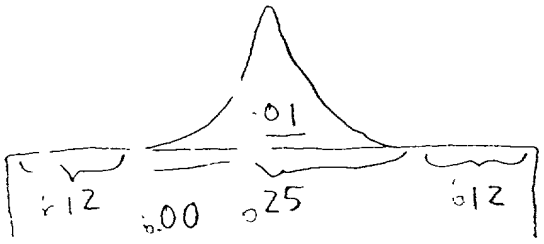

FIG.6A

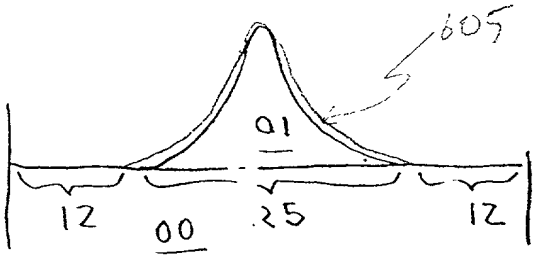

FIG. .6B

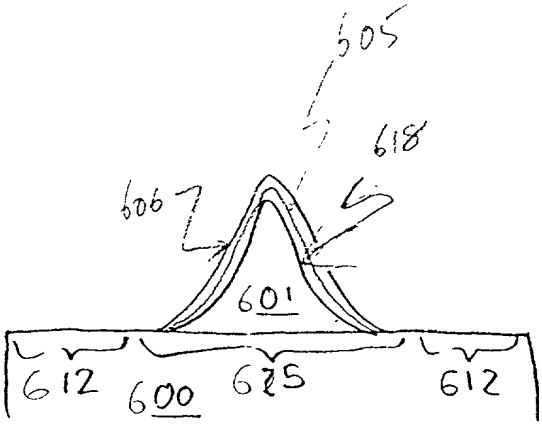

FIG. 6C

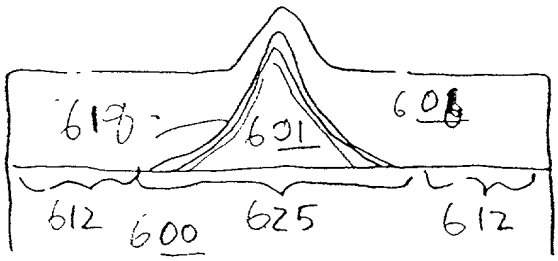

FIG. 6D

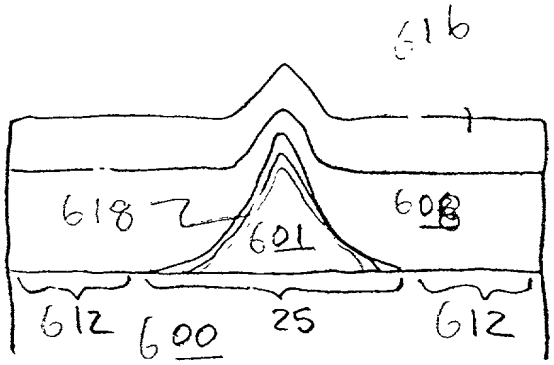

FIG. 6E

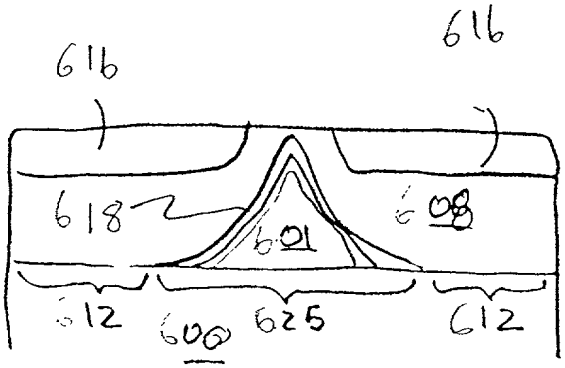

FIG. 6F

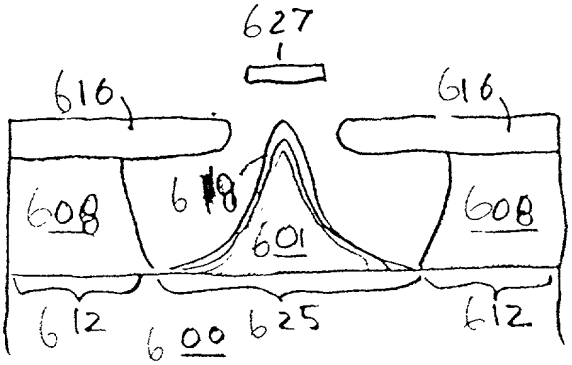

FIG 6G

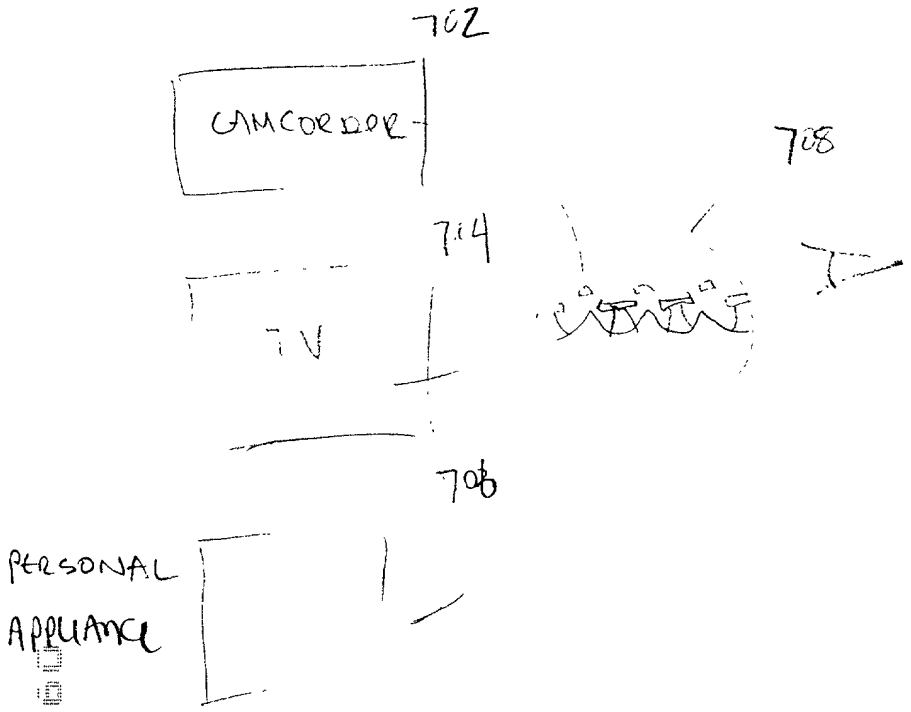
702
CAMCORDER
708
714
TV
706
PERSONAL
APPLIANCE

FIG. 7

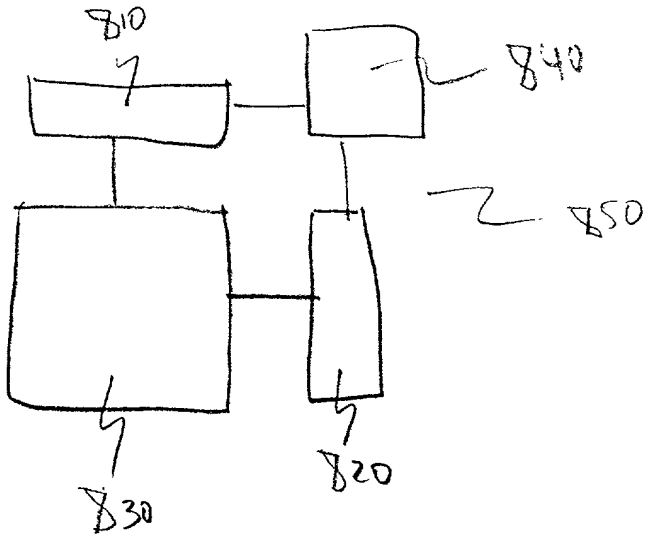
810
840
850
830
820

FIG. 8

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

DECLARATION FOR PATENT APPLICATION

As a below named inventor I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:

STRUCTURES AND METHODS TO ENHANCE FIELD EMISSION IN FIELD EMITTER DEVICES .

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56 (see page 3 attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, §119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

No such claim for priority is being made at this time.

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below:

No such claim for priority is being made at this time.

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application.

No such claim for priority is being made at this time.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of sole inventor : **Yongjun Hu**
Citizenship: **Peoples Republic of China** Residence: **Boise, ID**
Post Office Address: 2470 Canal St., #203
Boise, ID 83705

Signature: _____ Date: 08/27/98
Yongjun Hu

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) it establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) it refutes, or is inconsistent with, a position the applicant takes in:

(i) opposing an argument of unpatentability relied on by the Office, or

(ii) asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.